UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,175	06/24/2003	Eugene B. Hinterscher	TI-36136	9443

23494 7590 06/29/2004

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,175	HINTERSCHER, EUGENE B.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3 and 4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3 and 4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is responsive to the amendment filed on 5/17/04.

2. The rejection under 35 U.S.C. 112, 2nd paragraph, of claim 4 in the last office action has been withdrawn based on applicant's clarification. However, based on applicant's explanation, it appears that the claim needs to be amended as suggested bellow.

Claim Objections

3. Claim 4 is objected to because of the following informalities: on line 1 of claim 4, it is suggested to changed "further comprising" to --wherein each of the upper and lower predriver circuits comprising--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ten Eyck (USP 6,137,322) in view of Lin (USP 6,552,594).

With respect to claims 3 and 4, Figure 1 of the Ten Eyck reference discloses an output circuit, which includes: a pull-up circuit (28) including an upper output transistor (28) connected between a power supply (38) and an output node (42); a pull-down circuit (22) including a lower output transistor (22) connected between ground (40) and the output node (42); an upper pre-driver circuit (23, 24, 26, 27) receiving an input signal (34) and provide a voltage at the gate of

the upper output transistor (28); and a lower pre-driver circuit (20, 21, 29, 30) receiving the input signal (34) and provide another voltage at the gate of the lower output transistor (22). The Ten Eyck reference does not disclose that the pull-up circuit including an upper damping control circuit connected between the upper output transistor and the output node, and the pull-down circuit including a lower damping control circuit connected between the lower output transistor and the output node, wherein the upper damping control circuit comprising a first diode and a first resistor connected in parallel, and wherein the lower damping control circuit comprising a second diode and the second resistor connected in parallel. However, the Lin reference discloses in Figure 11A an output circuit that includes a pull-up circuit (60) and a pull-down circuit (62), wherein the pull-up circuit (60) including a resistance modulator (the diode and resistor connected in parallel in the pull-up circuit 60 in Figure 11A) connected between the upper output transistor (P1) and the output node (64), and the pull-down circuit (62) including another resistance modulator (66) connected between the lower output transistor (N1) and the output node (64) for the purpose of suppress the voltage ringing and overshooting (lines 12-37 of Col. 6, and lines 11-24 of Col. 7). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 1 of the Ten Eyck reference by providing the output circuit in Figure 1 of the Ten Eyck reference with a first resistance modulator connected between the upper output transistor and the output node, and a second resistance modulator connected between the lower output transistor and the output node, wherein the first resistance modulator comprising a first diode and a first resistor connected in parallel, and the second resistance modulator comprising a second diode and the second resistor connected in parallel as taught in Figure 11A of the Lin reference for the purpose of voltage

ringing and overshooting suppression. Thus this modification/combination meets all the limitations of claims 1-4. Note that the upper damping circuit and the lower damping circuit are the first resistance modulator and the second resistance modulator, respectively. Also note that, in Figure 1 of the Ten Eyck reference, the upper and lower pre-driver circuits receive the tristate enable signal (36) for causing the output node (42) to be in a tristate condition in response the tristate enable input signal (36).

Response to Arguments

6. Applicant's arguments filed on 5/17/04 have been fully considered but they are not persuasive.

Applicant argues that "Lin fails to describe a lower damping control circuit branch, comprising a second resistor and a second diode connected in parallel between a third node and the second node, and a lower output transistor coupled by its source and drain between ground and the third node, and having a gate. Lin's diode D1 and resistor Rn are not connected in parallel between a third node and an output node, wherein a lower output transistor is connected between the third node and ground, as recited in claim 3, because their NMOS device N1 is not an output transistor". However, this argument is not persuasive. Note that the lower damping circuit is 62 in Figure 11A of Lin (which is similar as 30 in Figure 2). It is clearly (from Figure 2 of Lin) Rn and D1 is connected in parallel between Pad 38 (second node) and the junction of Rn and N1 (third node), and N1 is connected between the third node and ground. The Lin reference (lines 25-28 of Col. 4) also discloses that circuit 30 is buffer circuit which pull-low during the operation (i.e., depend on the signal applies to the gate of N1, buffer circuit 30 pull node 38 to low), so it is reasonable to construe that pad node 38 is the output node of buffer 30. Because the

all of structure elements of the claims are met and the Examiner also provides a motivation of the combination, therefore the rejections of claims 3 and 4 are proper.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 24, 2004

Long Nguyen
Primary Examiner
Art Unit: 2816